REMARKS

This AMENDMENT UNDER 37 CFR 1.111 is filed in reply to the outstanding Office Action of June 5, 2003, and is believed to be fully responsive thereto for reasons set forth below in greater detail.

Responsive to paragraphs 2 and 3 of the Office Action, the specification has been amended to correct the noted errors. Regarding paragraph 3, the error was in the specification, not the drawings.

Reconsideration is respectfully requested of the rejection of claims 1-4 as being allegedly obvious over Platko et al, particularly in view of the clarifying amendments to independent claims 1, 3 and 4 requested herein and the following comments on the distinctions of the present invention over Platko.

The Present Invention Compared to Platko

The problem that the present invention seeks to solve is to allow a master processor to access a high latency memory without stalling the processor. The solution is to use a slave processor to access the memory, freeing the master processor to continue other processing operations and tasks while the slave processor accesses the memory. The slave processor then posts the results of the reads to the master processor later.

The cited prior art Platko interfaces a slave processor (e.g. encryption engine) to an ASIC (master processor) at a lower cost, by reusing the memory bus and employing some extra signals. Reusing the memory bus reduces the number of pins consumed on the ASIC.

However, the Platko reference does not allow the master processor to continue other processing operations and tasks while the slave processor is reading the memory; indeed, Platko requires that the master processor in one scenario actually drive the reads that generate data onto the memory bus, and then further drives the writes that put the data into the slave

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processor, and in another scenario use reads and writes to transfer the data from slave processor to memory.

Though the same terms are used in the present invention and Platko, the "master processor" in the present invention is very different from the "master processor" in the prior art Platko reference which is actually an ASIC with custom logic. Only a portion of this custom logic need be involved in data transfers, and it is therefore relatively inexpensive to stall in marshalling these data transfers. The "master processor" in the present invention is a high performance processor which is entirely consumed while waiting for the data transfer, and is therefore expensive.

So, a key difference is that the master processor of the present invention is able to continue processing operations while the read is being performed by the slave processor.

Those features of the present invention are mentioned in the specification at page 8, lines 12-13, "In the meantime the processor is free to perform other tasks," and at page 11, lines 15-21, "Advantageously, the master processor 10 does not then have to wait or otherwise stall until the requested data is returned from the memory 50. This is because the master processor 10 has effectively delegated execution of the read request to the slave processor 20. The slave processor 30 absorbs any waiting, stalling or other latency associated with the memory access."
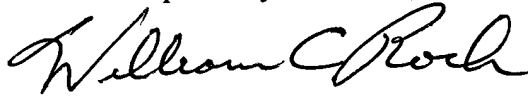
In the cited prior art reference Platko, the master processor is synchronously sequencing the operation of the slave processor. Whereas, in the present invention, the master processor is sending an asynchronous request to the slave processor and the slave processor is coming back with an asynchronous reply.

The present invention avoids stalling the master processor while the asynchronous memory read is in progress.

Independent claims 1, 3 and 4 have been amended to clarify the above distinctions of the present invention over Platko.

This application is now believed to be in condition for allowance, a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

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